EAST SEARCH

10/16/04

L#	Hits	Search String	Databases
L1	20776	register and port and allocat$5	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L2	3201	register same (port and allocat$5)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L3	929	2 and (instruction same (parallel$5 and processor))	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L4	877	register same (port and allocat$5 and instruction and parallel$5 and processor)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB
L5	699	register same (port and allocat$5 and instruction and parallel$5 and processor)	USPAT; EPO; JPO; DERWENT; IBM_TDB
L6	139	5 and (port near5 shar$5)	USPAT; EPO; JPO; DERWENT; IBM_TDB

Results of search set L6:

US 6801997 B2	Multiple-thread processor with single-thread interface shared among threads	20041005	712/229
US 6735690 B1	Specifying different type generalized event and action pair in a processor	20040511	712/244
US 6694347 B2	Switching method in a multi-threaded processor	20040217	718/108
US 6691301 B2	System, method and article of manufacture for signal constructs in a programming language capable of programming hardware architectures	20040210	717/114
US 6691240 B1	System and method of implementing variabe length delay instructions, which prevents overlapping lifetime information or values in efficient way	20040210	713/400
US 6651222 B2	Automatic design of VLIW processors	20031118	716/1
US 6629312 B1	Programmatic synthesis of a machine description for retargeting a compiler	20030930	717/136
US 6629187 B1	Cache memory controlled by system address properties	20030930	711/3
US 6609163 B1	Multi-channel serial port with programmable features	20030819	710/21
US 6594728 B1	Cache memory with dual-way arrays and multiplexed parallel output	20030715	711/127
US 6581187 B2	Automatic design of VLIW processors	20030617	716/1
US 6542991 B1	Multiple-thread processor with single-thread interface shared among threads	20030401	712/228
US 6507947 B1	Programmatic synthesis of processor element arrays	20030114	717/160
US 6507862 B1	Switching method in a multi-threaded processor	20030114	718/107
US 6499123 B1	Method and apparatus for debugging an integrated circuit	20021224	714/724
US 6496940 B1	Multiple processor system with standby sparing	20021217	714/4
US 6457173 B1	Automatic design of VLIW instruction formats	20020924	717/149
US 6408428 B1	Automated design of processor systems using feedback from internal measurements of candidate systems	20020618	716/17
US 6408375 B2	System and method for register renaming	20020618	712/23
US 6385757 B1	Auto design of VLIW processors	20020507	716/1

US 6351808 B1	Vertically and horizontally threaded processor with multidimensional storage for storing thread data	20020226	712/228
US 6333938 B1	Method and system for extracting control information from packetized data received by a communications interface device	20011225	370/503
US 6311261 B1	Apparatus and method for improving superscalar processors	20011030	712/23
US 6282583 B1	Method and apparatus for memory access in a matrix processor computer	20010828	709/400
US 6275920 B1	Mesh connected computed	20010814	712/14
US 6272617 B1	System and method for register renaming	20010807	712/23
US 6233702 B1	Self-checked, lock step processor pairs	20010515	714/48
US 6216200 B1	Address queue	20010410	711/100
US 6212629 B1	Method and apparatus for executing string instructions	20010403	712/241
US 6212628 B1	Mesh connected computer	20010403	712/226
US 6205223 B1	Input data format autodetection systems and methods	20010320	380/42
US 6195676 B1	Method and apparatus for user side scheduling in a multiprocessor operating system program that implements distributive scheduling of processes	20010227	718/107
US 6179489 B1	Devices, methods, systems and software products for coordination of computer main microprocessor and second microprocessor coupled thereto	20010130	718/102
US 6173388 B1	Directly accessing local memories of array processors for improved real-time corner turning processing	20010109	712/22
US 6161208 A	Storage subsystem including an error correcting cache and means for performing memory to memory transfers	20001212	714/764
US 6157967 A	Method of data communication flow control in a data processing system using busy/ready commands	20001205	710/19
US 6151689 A	Detecting and isolating errors occurring in data communication in a multiple processor system	20001121	714/49
US 6148391 A	System for simultaneously accessing one or more stack elements by multiple functional units using real stack addresses	20001114	712/202
US 6138231 A	System and method for register renaming	20001024	712/216
US 6112019 A	Distributed instruction queue	20000829	712/214
US 6085275 A	Data processing system and method thereof	20000704	710/316
US 6081852 A	Packet data transferring system for autonomously operating a DMA by autonomous boot mode select signal wherein the DMA is enabled to at least one program control list	20000627	710/24
US 6081783 A	Dual processor digital audio decoder with shared memory data transfer and task partitioning for decompressing compressed audio data, and systems and methods using the same	20000627	704/500
US 6065107 A	System for restoring register data in a pipelined data processing system using latch feedback assemblies	20000516	712/32
US 6052773 A	DPGA-coupled microprocessors	20000418	712/43
US 6044451 A	VLIW processor with write control unit for allowing less write buses than functional units	20000328	712/24

US 6012135 A	Computer having multiple address ports, each having logical address translation with base and limit memory management	20000104	711/208
US 6006286 A	System for controlling data packet transfers by associating plurality of data packet transfer control instructions in packet control list including plurality of related logical functions	19991221	710/22
US 5996032 A	System for writing a plurality of data bits less than from the total number of bits in a data register using a single register write operation	19991130	710/62
US 5983301 A	Method and system for assigning a direct memory access priority in a packetized data communications interface device	19991109	710/113
US 5964835 A	Storage access validation to data messages using partial storage address data indexed entries containing permissible address range validation for message source	19991012	709/216
US 5963746 A	Fully distributed processing memory element	19991005	712/20
US 5963745 A	APAP I/O programmable router	19991005	712/13
US 5963543 A	Error detection and correction apparatus for an asynchronous transfer mode (ATM) network device	19991005	370/232
US 5948080 A	System for assigning a received data packet to a data communications channel by comparing portion of data packet to predetermined match set to check correspondence for directing channel select signal	19990907	710/37
US 5933855 A	Shared, reconfigurable memory architectures for digital signal processing	19990803	711/200
US 5931939 A	Read crossbar elimination in a VLIW processor	19990803	712/24
US 5914953 A	Network message routing using routing table information and supplemental enable information for deadlock prevention	19990622	370/392
US 5909559 A	Bus bridge device including data bus of first width for a first processor, memory controller, arbiter circuit and second processor having a different second data width	19990601	710/307
US 5875346 A	System for restoring register data in a pipelined data processing system using latch feedback assemblies	19990223	712/1
US 5867501 A	Encoding for communicating data and commands	19990202	370/474
US 5842036 A	Circuit and method for scheduling instructions by predicting future availability of resources required for execution	19981124	712/23
US 5842031 A	Advanced parallel array processor (APAP)	19981124	712/23
US 5838904 A	Random number generating apparatus for an interface unit of a carrier sense with multiple access and collision detect (CSMA/CD) ethernet data network	19981117	709/250
US 5838894 A	Logical, fail-functional, dual central processor units formed from three processor units	19981117	714/11
US 5809325 A	Circuit and method for scheduling instructions by predicting future availability of resources required for execution	19980915	712/32
US 5805909 A	Microprocessors or microcontroller utilizing FLL clock having a reduced power state	19980908	713/322
US 5805906 A	Method and apparatus for writing information to registers in a data processing system using a number of registers for processing instructions	19980908	710/260

US 5805874 A	Method and apparatus for performing a vector skip instruction in a data processor	19980908	712/222
US 5802287 A	Single chip universal protocol multi-function ATM network interface	19980901	370/395.5
US 5794059 A	N-dimensional modified hypercube	19980811	712/10
US 5793944 A	System for restoring register data in a pipelined data processing system using register file save/restore mechanism	19980811	714/15
US 5790776 A	Apparatus for detecting divergence between a pair of duplexed, synchronized processor elements	19980804	714/10
US 5781753 A	Semi-autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for speculative and out-of-order execution of complex instructions	19980714	712/218
US 5768575 A	Semi-Autonomous RISC pipelines for overlapped execution of RISC-like instructions within the multiple superscalar execution units of a processor having distributed pipeline control for sepculative and out-of-order execution of complex instructions	19980616	712/228
US 5758112 A	Pipeline processor with enhanced method and apparatus for restoring register-renaming information in the event of a branch misprediction	19980526	712/217
US 5754805 A	Instruction in a data processing system utilizing extension bits and method therefor	19980519	712/200
US 5752074 A	Data processing system and method thereof	19980512	712/29
US 5752070 A	Asynchronous processors	19980512	712/33
US 5751955 A	Method of synchronizing a pair of central processor units for duplex, lock-step operation by copying data into a corresponding locations of another memory	19980512	714/12
US 5751932 A	Fail-fast, fail-functional, fault-tolerant multiprocessor system	19980512	714/12
US 5742786 A	Method and apparatus for storing vector data in multiple non-consecutive locations in a data processor using a mask value	19980421	711/217
US 5740404 A	Digital signal processor with on-chip select decoder and wait state generator	19980414	711/167
US 5737586 A	Data processing system and method thereof	19980407	712/236
US 5734921 A	Advanced parallel array processor computer package	19980331	712/10
US 5734879 A	Saturation instruction in a data processor	19980331	712/221
US 5717947 A	Data processing system and method thereof	19980210	712/3
US 5717943 A	Advanced parallel array processor (APAP)	19980210	712/20
US 5717895 A	Associative scalar data cache with write-through capabilities for a vector processor	19980210	711/140
US 5710935 A	Advanced parallel array processor (APAP)	19980120	712/20
US 5706488 A	Data processing system and method thereof	19980106	712/223
US 5689689 A	Clock circuits for synchronized processor systems having clock generator circuit with a voltage control oscillator producing a clock signal synchronous with a master clock signal	19971118	709/400

US 5675807 A	Interrupt message delivery identified by storage location of received interrupt data	19971007	710/260
US 5675579 A	Method for verifying responses to messages using a barrier message	19971007	370/248
US 5668809 A	Single chip network hub with dynamic window filter	19970916	370/392
US 5664134 A	Data processor for performing a comparison instruction using selective enablement and wired boolean logic	19970902	712/245
US 5654962 A	Error detection and correction method for an asynchronous transfer mode (ATM) network device	19970805	370/232
US 5640399 A	Single chip network router	19970617	370/392
US 5625836 A	SIMD/MIMD processing memory element (PME)	19970429	709/214
US 5625825 A	Random number generating apparatus for an interface unit of a carrier sense with multiple access and collision detect (CSMA/CD) ethernet data network	19970429	710/242
US 5600846 A	Data processing system and method thereof	19970204	712/5
US 5598571 A	Data processor for conditionally modifying extension bits in response to data processing instruction execution	19970128	712/9
US 5590345 A	Advanced parallel array processor(APAP)	19961231	712/11
US 5588152 A	Advanced parallel processor including advanced support hardware	19961224	712/16
US 5574849 A	Synchronized data transmission between elements of a processing system	19961112	714/12
US 5572689 A	Data processing system and method thereof	19961105	712/200
US 5561784 A	Interleaved memory access system having variable-sized segments logical address spaces and means for dividing/mapping physical address into higher and lower order addresses	19961001	711/157
US 5559973 A	Data processing system and method thereof	19960924	712/241
US 5555432 A	Circuit and method for scheduling instructions by predicting future availability of resources required for execution	19960910	712/23
US 5548768 A	Data processing system and method thereof	19960820	712/200
US 5537562 A	Data processing system and method thereof	19960716	712/234
US 5524255 A	Method and apparatus for accessing global registers in a multiprocessor system	19960604	712/203
US 5471593 A	Computer processor with an efficient means of executing many instructions simultaneously	19951128	712/235
US 5446726 A	Error detection and correction apparatus for an asynchronous transfer mode (ATM) network device	19950829	370/232
US 5428754 A	Computer system with clock shared between processors executing separate instruction streams	19950627	712/220
US 5329630 A	System and method using double-buffer preview mode	19940712	711/173
US 5276848 A	Shared two level cache including apparatus for maintaining storage consistency	19940104	711/121
US 5261059 A	Crossbar interface for data communication network	19931109	710/317
US 5202972 A	Store buffer apparatus in a multiprocessor system	19930413	711/123
US 5197130 A	Cluster architecture for a highly parallel scalar/vector multiprocessor system	19930323	712/3

US 5185872 A	System for executing different cycle instructions by selectively bypassing scoreboard register and canceling the execution of conditionally issued instruction if needed resources are busy	19930209	712/217
US 5179702 A	System and method for controlling a highly parallel multiprocessor using an anarchy based scheduler for parallel execution thread scheduling	19930112	718/102
US 5175856 A	Computer with integrated hierarchical representation (IHR) of program wherein IHR file is available for debugging and optimizing during target execution	19921229	717/151
US 5168547 A	Distributed architecture for input/output for a multiprocessor system	19921201	710/1
US 5165038 A	Global registers for a multiprocessor system	19921117	711/147
US 5056015 A	Architectures for serial or parallel loading of writable control store	19911008	703/27
US 5048012 A	Data link controller with flexible multiplexer	19910910	370/498
US 5042000 A	Integral transform method	19910820	708/404
US 5023776 A	Store queue for a tightly coupled multiple processor configuration with two-level cache buffer storage	19910611	711/122
US 4949333 A	Enhanced universal asynchronous receiver-transmitter	19900814	370/282
US 4907225 A	Data protocol controller	19900306	370/463
US 4901230 A	Computer vector multiprocessing control with multiple access memory and priority conflict resolution method	19900213	711/149
US 4852088 A	Packet-at-a-time reporting in a data link controller	19890725	370/413
US 4809269 A	Dual-port timing controller	19890228	370/462
US 4661900 A	Flexible chaining in vector processor with selective use of vector registers as operand and result registers	19870428	712/4
US 4636942 A	Computer vector multiprocessing control	19870113	710/269
US 4491916 A	Large volume, high speed data processor	19850101	710/107
US 4400778 A	Large-volume, high-speed data processor	19830823	710/1
NN85057075	Grouped Multiprocessor Architecture	19850501	

Welcome to IEEE Xplore®
- Home
- What Can I Access?
- Log-out

Tables of Contents
- Journals & Magazines
- Conference Proceedings
- Standards

Search
- By Author
- Basic
- Advanced

Member Services
- Join IEEE
- Establish IEEE Web Account
- Access the IEEE Member Digital Library

Print Format

Your search matched **23** of **991547** documents.

A maximum of **23** results are displayed, **50** to a page, sorted by **publication year** in **ascending** order.
You may refine your search by editing the current search expression or entering a new one the text box.
Then click **Search Again.**

register* and port* and alloc* Search Again

Results:
Journal or Magazine = **JNL** Conference = **CNF** Standard = **STD**

1 **Provisions for High Frequency Future Use**
Feigleson, H.;
Communications, IEEE Transactions on [legacy, pre - 1988] , Volume: 29 Issue: 8 , Aug 1981
Page(s): 1156 -1160

[Abstract] [PDF Full-Text (552 KB)] **IEEE JNL**

2 **Optimal allocation of multiport memories in datapath synthesis**
Wilson, T.C.; Banerji, D.K.; Majithia, J.C.; Majumdar, A.K.;
Circuits and Systems, 1989., Proceedings of the 32nd Midwest Symposium on , 14-16 Aug. 1989
Page(s): 1070 -1073 vol.2

[Abstract] [PDF Full-Text (300 KB)] **IEEE CNF**

3 **An efficient register allocation for a WAM PROLOG compiler**
Ku, F.P.; Cheung, Y.S.; Tse, K.W.;
TENCON 90. 1990 IEEE Region 10 Conference on Computer and Communication Systems , 24-27 Sept. 1990
Page(s): 702 -712 vol.2

[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

4 **Compiling multi-dimensional data streams into distributed DSP ASIC memory**
Vanhoof, J.; Bolsens, I.; De Man, H.;
Computer-Aided Design, 1991. ICCAD-91. Digest of Technical Papers., 1991 IEEE International Conference on , 11-14 Nov. 1991
Page(s): 272 -275

[Abstract] [PDF Full-Text (312 KB)] **IEEE CNF**

---

5 **Allocation of multiport memory with ports of different type in register transfer level synthesis**
Chen, C.-I.H.;
Computer Design: VLSI in Computers and Processors, 1991. ICCD '91. Proceedings., 1991 IEEE International Conference on , 14-16 Oct. 1991
Page(s): 418 -421

[Abstract] [PDF Full-Text (344 KB)] **IEEE CNF**

---

6 **Program structure as basis for parallelizing global register allocation**
Zobel, A.;
Computer Languages, 1992., Proceedings of the 1992 International Conference on , 20-23 April 1992
Page(s): 262 -271

[Abstract] [PDF Full-Text (780 KB)] **IEEE CNF**

---

7 **A stochastic evolution based register allocation using multiport memories**
Varadarajan, S.; Ramakrishna, N.A.; Bayoumi, M.A.;
Circuits and Systems, 1993., Proceedings of the 36th Midwest Symposium on , 16-18 Aug. 1993
Page(s): 472 -475 vol.1

[Abstract] [PDF Full-Text (288 KB)] **IEEE CNF**

---

8 **Datapath synthesis using onchip multiport memories**
Ahmad, I.; Chen, C.Y.R.;
Computers and Digital Techniques, IEE Proceedings E [see also Computers and Digital Techniques, IEE Proceedings-] , Volume: 140 Issue: 4 , July 1993
Page(s): 227 -232

[Abstract] [PDF Full-Text (388 KB)] **IEE JNL**

---

9 **Low power data format converter design using semi-static register allocation**
Srivatsan, K.; Chakrabarti, C.; Lucke, L.;
Computer Design: VLSI in Computers and Processors, 1995. ICCD '95. Proceedings., 1995 IEEE International Conference on , 2-4 Oct. 1995
Page(s): 460 -465

[Abstract] [PDF Full-Text (496 KB)] **IEEE CNF**

10 **Data path synthesis in digital electronics. I. Memory allocation**
Chen, C.H.;
Aerospace and Electronic Systems, IEEE Transactions on , Volume: 32 Issue: 1 , Jan. 1996
Page(s): 2 -15

[Abstract] [PDF Full-Text (1064 KB)] **IEEE JNL**

11 **An algorithm based on the Hungarian method for register reduction during complex functional unit allocation**
Ta-Cheng Lin; Cyre, W.R.;
Southeastcon '97. 'Engineering new New Century'., Proceedings. IEEE , 12-14 April 1997
Page(s): 43 -47

[Abstract] [PDF Full-Text (464 KB)] **IEEE CNF**

12 **A graph-theoretic approach for register file based synthesis**
Ravikumar, C.P.; Aggarwal, R.; Sharma, C.;
VLSI Design, 1997. Proceedings., Tenth International Conference on , 4-7 Jan. 1997
Page(s): 118 -123

[Abstract] [PDF Full-Text (500 KB)] **IEEE CNF**

13 **Performing scheduling and storage optimization simultaneously using genetic algorithms**
Torbey, E.; Knight, J.;
Circuits and Systems, 1998. Proceedings. 1998 Midwest Symposium on , 9-12 Aug. 1998
Page(s): 284 -287

[Abstract] [PDF Full-Text (756 KB)] **IEEE CNF**

14 **A novel renaming scheme to exploit value temporal locality through physical register reuse and unification**
Jourdan, S.; Ronen, R.; Bekerman, M.; Shomar, B.; Yoaz, A.;
Microarchitecture, 1998. MICRO-31. Proceedings. 31st Annual ACM/IEEE International Symposium on , 30 Nov.-2 Dec. 1998
Page(s): 216 -225

[Abstract] [PDF Full-Text (128 KB)] **IEEE CNF**

15 **Decreasing process memory requirements by overlapping program portions**
Bowman, R.L.; Ratliff, E.J.; Whalley, D.B.;
System Sciences, 1998., Proceedings of the Thirty-First Hawaii International Conference on , Volume: 7 , 6-9 Jan. 1998
Page(s): 115 -124 vol.7

[Abstract] [PDF Full-Text (168 KB)] **IEEE CNF**

---

16 **A simple analytical framework for location management in personal communication systems**
Tonguz, O.K.; Mishra, S.; Hanwook Jung;
Vehicular Technology, IEEE Transactions on , Volume: 47 Issue: 2 , May 1998
Page(s): 428 -439

[Abstract] [PDF Full-Text (260 KB)] **IEEE JNL**

---

17 **A DRAM system for consistently reducing CPU wait cycles**
Kanno, Y.; Mizuno, H.; Watanabe, T.;
VLSI Circuits, 1999. Digest of Technical Papers. 1999 Symposium on , 17-19 June 1999
Page(s): 131 -132

[Abstract] [PDF Full-Text (188 KB)] **IEEE CNF**

---

18 **Heuristic tradeoffs between latency and energy consumption in register assignment**
Anand, R.; Jacome, M.; De Veciana, G.;
Hardware/Software Codesign, 2000. CODES 2000. Proceedings of the Eighth International Workshop on , 3-5 May 2000
Page(s): 115 -119

[Abstract] [PDF Full-Text (548 KB)] **IEEE CNF**

---

19 **An integrated data path optimization for low power based on network flow method**
Chun-Gi Lyuh; Taewhan Kim; Liu, C.L.;
Computer Aided Design, 2001. ICCAD 2001. IEEE/ACM International Conference on , 4-8 Nov. 2001
Page(s): 553 -559

[Abstract] [PDF Full-Text (716 KB)] **IEEE CNF**

---

20 **Estimation of lower and upper bounds on the power consumption from scheduled data flow graphs**
Kruse, L.; Schmidt, E.; Jochens, G.; Stammermann, A.; Schulz, A.; Macii, E.; Nebel, W.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9
Issue: 1 , Feb. 2001
Page(s): 3 -14

[Abstract] [PDF Full-Text (292 KB)] **IEEE JNL**

---

21 **Register write specialization register read specialization: a path to complexity-effective wide-issue superscalar processors**
Seznec, A.; Toullec, E.; Rochecouste, O.;
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on , 18-22 Nov. 2002
Page(s): 383 -394

[Abstract] [PDF Full-Text (294 KB)] **IEEE CNF**

---

22 **Reducing register ports for higher speed and lower energy**
Park, I.; Powell, M.D.; Vijaykumar, T.N.;
Microarchitecture, 2002. (MICRO-35). Proceedings. 35th Annual IEEE/ACM International Symposium on , 18-22 Nov. 2002
Page(s): 171 -182

[Abstract] [PDF Full-Text (277 KB)] **IEEE CNF**

---

23 **Scheme for reducing size of coefficient memory in FFT processor**
Hasan, M.; Arslan, T.;
Electronics Letters , Volume: 38 Issue: 4 , 14 Feb 2002
Page(s): 163 -164

[Abstract] [PDF Full-Text (287 KB)] **IEE JNL**
